AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (currently amended) A method for a processor to process a ~~processing a compressed~~ sequence of a plurality of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for [[an]] a corresponding element of [[a]] the processor, the method comprising:

fetching an identifier ~~that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words~~ having one bit for each element of the processor, wherein a bit of the identifier is set if a corresponding ordered field contains a NOP instruction in every control word of the sequence of control words;

disabling an element of the processor, to reduce power consumption by the processor, if a corresponding bit of the identifier is set; and, while the element is disabled:

for each control word of the ~~compressed~~ sequence of multiple-instruction control words;

fetching a control word;

~~reconstructing a corresponding uncompressed control word by inserting NOP instructions into the compressed control word in accordance with the identifier;~~

~~providing the decompressed control word to the processor for execution; and~~

the processor executing the ~~decompressed~~ control word.

7. (currently) A method in accordance with claim 6, wherein the processor further comprises a plurality of memory banks each associated with an element of a processor, the method further comprising:

disabling a memory bank of the plurality of memory banks while the sequence of control words is processed, to reduce power consumption by the processor further, if a corresponding bit of the identifier is set;

enabling other memory banks ~~a subset~~ of the plurality of memory banks ~~sufficient to store one or more control words of the compressed sequence of multiple-instruction control words in accordance with the identifie~~;and

~~disabling other memory banks of the plurality of memory banks; and~~

for each control word of the ~~compressed~~ sequence of control words:

storing the control word in the enabled subset of memory banks.

8. (cancelled)

9. (cancelled)

10. (currently amended) A system for processing a compressed sequence of a plurality of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for an element of a processor, the system comprising:

a mask latch for storing a compression mask ~~that identifies a set of aligned fields removed during compression of the sequence of multiple-instruction control words~~ having one bit for each element of the processor, wherein a bit of the compression mask is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of control words;

a logic unit coupled to the mask latch and responsive to the compression mask;

a memory for storing one or more compressed multiple-instruction control words;

a pipelined permute unit, coupled to the logic unit and the memory and operable to reconstruct multiple-instruction control words by fetching a compressed multiple-instruction control word from the memory and inserting NOP instructions in accordance with the compression mask; and

an instruction register, coupled the pipelined permute unit and operable to present reconstructed multiple-instruction control words to the processor.

11. (currently amended) A system in accordance with claim 10, wherein the memory comprises a plurality of memory banks coupled to the logic unit, and wherein the logic unit is operable to disable memory banks in accordance with the compression mask, the memory banks remaining disabled while the sequence of control words is processed.

12. (currently amended) A system in accordance with claim 10, further comprising:

a plurality of processing elements coupled to the mask latch and the instruction register and controlled by the reconstructed multiple-instruction control words,

wherein the compression mask is used to disable[[d]] processing elements of the plurality of processing elements that are unused by all control words of the

sequence of multiple-instruction control words.

13. (original) A system in accordance with claim 12, wherein the plurality of processing elements form part of a re-configurable streaming vector processor, and wherein the sequence of multiple-instruction control words is a sequence of VLIWs describing a dataflow graph.

14. (new) A system for processing a sequence of a plurality of multiple-instruction control words, each control word comprising a plurality of ordered fields and each ordered field containing an instruction for a datapath element of a processor, the system comprising:

a mask latch for storing a bit mask having one bit for each datapath element, wherein a bit of the bit mask is set if a corresponding ordered field contains a NOP instruction in every multiple-instruction control word of the sequence of control words;

a plurality of memory banks operable to store instructions of a multiple-instruction control word;

a plurality of datapath elements;

a logic unit coupled to the mask latch, the memory banks and the datapath elements and operable to enable and disable the plurality of memory banks and the plurality of datapath elements, in accordance

with the bit mask, before the sequence of control words is processed; and

an instruction register, coupled to the memory banks and operable to present instructions the datapath elements.

15. (new) A system in accordance with claim 14, wherein the plurality of datapath elements form part of a re-configurable streaming vector processor, and wherein the sequence of a plurality multiple-instruction control words is a sequence of VLIWs describing a dataflow graph.